In the claims:

1. A method of writing to a memory array comprising a plurality of three terminal memory cells, the method comprising:

applying a write voltage to a selected memory cell, the write voltage diffusing conductive elements through the selected memory cell and changing a capacitance of the memory cell.

2. The method of claim 1, wherein the step of applying a write voltage comprises:

applying a voltage to a gate electrode of the selected memory cell.

3. The method of claim 2, wherein the step of applying a write voltage comprises:

applying a medium voltage to unselected data lines in the memory array; and

applying the medium voltage to unselected gate lines in the memory array.

4. The method of claim 2, wherein the selected memory cell includes a gate insulator, the step of applying a write voltage comprising:

applying a write voltage sufficient to diffuse conductive elements of the gate electrode through the gate insulator.

5. The method of claim 4, wherein the selected memory cell includes at least one floating gate adjacent to the gate insulator, the step of applying a write voltage comprising:

diffusing the conductive elements through the insulator so that the conductive elements form a conductive path from the gate electrode to the floating gate.

6. The method of claim 2, wherein the selected memory cell comprises a plurality of floating gates, the step of applying a write voltage comprising:

applying one of at least two write voltages to diffuse conductive elements from one floating gate to another floating gate.

7. A memory cell, comprising:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

8. The memory cell of claim 7, wherein the channel region, the source, and the drain are parts of a continuous layer of semiconductor material.

9. The memory cell of claim 8, wherein the source and drain are doped regions of the layer of semiconductor material.

10. The memory cell of claim 7, wherein the gate insulator extends between the diffusive metal and the floating gate, and between the floating gate and the channel region.

11. The memory cell of claim 10, wherein the diffusive metal is a gate electrode.

12. The memory cell of claim 7, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.

13. A memory array, comprising:

a substrate;

a plurality of gate lines disposed over the substrate;

a plurality of data lines crossing the gate lines and disposed over the substrate; and

a plurality of memory cells at crossing points of the gate lines and data lines, each memory cell being coupled to a gate line and a data line that cross at the memory cell, wherein a memory cell comprises:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

14. The memory array of claim 13, wherein the data lines comprise strips of semiconductor material, the sources and the drains comprising doped regions of the data lines.

15. The memory array of claim 13, wherein the gate insulator extends between the diffusive metal and the floating gate, and between the floating gate and the channel region.

16. The memory array of claim 13, wherein the gate lines are conductive lines coupled to the memory cells, the diffusive metal comprising a part of a gate line.

17. The memory array of claim 13, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.

18. The memory array of claim 13, wherein the gate lines comprise:

a first conductor disposed over the gate insulator; and

a second conductor coupled to the first conductor.

19. The memory array of claim 18, wherein the first conductor includes a diffusive metal disposed between the insulator and the second conductor.

20. The memory array of claim 13, wherein the substrate comprises at least one of a glass or a plastic.

21. A method of making a memory array, comprising:

providing a substrate;

forming a semiconductor layer over the substrate;

forming strips from the semiconductor layer;

forming an insulator over the strips;

forming a gate layer over the insulator;

patterning the gate layer and the insulator using a mask;

forming source/drains using the mask; and

forming gate lines over the insulator, wherein the gate lines comprise diffusive metal or are electrically coupled to a diffusive metal gate electrode.

22. The method of claim 21, wherein the step of forming source/drains comprises:

doping exposed regions of the semiconductor layer using the mask as a doping mask.

23. The method of claim 21, wherein the step of forming gate lines comprises the step of:

forming gate lines comprising a diffusive metal over the insulator.

24. The method of claim 21, comprising:

forming electrodes over the insulator, the electrodes comprising a diffusive metal.

25. The method of claim 21, wherein the step of providing a substrate comprises:

providing a substrate comprising one of a glass or a plastic.